REMARKS

The present Amendment places objected-to claims 3-7 in independent form. As a result, it is respectfully submitted that these claims are now in condition for immediate allowance.

The present Amendment also revised independent claims 1 and 8 to refer to a "maximum" packet processing time that is "determined corresponding to packet length." This supported (for example) by the sentence at page 7 of the application, lines 21-23.

The present Amendment also adds two new dependant claims, 9 and 10. They are supported (for example) by Figure 1 of the present application's drawings, and by the description from the middle of page 7 of the specification through page 8.

The present application discloses an arrangement in which a packet processing time, representing a maximum time allowed for transmitting or receiving a packet, is divided into first and second parts (200A and 200B, as shown in Figure 2 of the application's drawings). During the first part, a first processing circuit (see reference number 10 in Figure 1 of the application's drawings) can access a storage circuit (reference number 12). During the second or residual part of the packet processing time, a second processing circuit (reference number 11) is permitted to access the storage circuit. The processing performed by the second processing circuit may comprise refreshing of the storage circuit.

The Office Action rejects independent claims 1 and 8 for obviousness on the basis of U.S. patent 6,338,108 to Motomura in view of U.S. patent 3,748,651 to Mesnik. For the reasons discussed below, however, it is respectfully submitted that the inventions now defined by claims 1 and 8 are patentable over these references.

The Motomura reference is directed to a large-scale memory using what the reference calls a packet-type memory bus. The Office Action calls attention to Motomura's Figure 9, and in particular to Motomura's DRAM 1 and his microprocessor 9 (characterized as a first processing circuit in the Office Action).

The Office Action acknowledges that Motomura fails to teach the "second processing circuit" of the independent claims, but takes the position that the Mesnik reference teaches first and second processing circuits connected to a storage device (Mesnik's elements 20 and 26) and means for allocating a first time period and a second time period. The Office Action then concludes that it would have been obvious for an ordinarily skilled person to modify Motomura's arrangement in accordance with Mesnik so as to achieve what is claimed. It should come as no surprise that Applicant respectfully disagrees with this conclusion.

The Mesnik references directed to an arrangement for refreshing a DRAM. Perhaps an ordinarily skilled person might consider using Mesnik's refreshing scheme with the DRAMs 1 that are shown in Motomura's Figure 9A. However, the result would still be what is shown in Motomura's Figure 9A: two DRAMs 1 and a microprocessor 9 connected to a bus 2. This is not what is recited in the independent claims.

Section 5 of the Office Action notes a passage in column 1 of the Mesnik reference. This passage observes that several different modes exist for refreshing a memory. One mode is to lengthen a read or write cycle and to refresh the memory at the end of the cycle.

Claim 1 now recites an allocation circuit that executes access time allocation with respect to "a maximum packet processing time allowed for processing each of said packets and determined corresponding to packet length", with a first time period of this maximum processing time being allocated to a first processing circuit to access a storage circuit and with a second time period of the maximum packet processing time being allocated to a second processing circuit to access the storage circuit. However, extending a read or write cycle in order to permit time for a refresh operation, in accordance with the Mesnik reference, would not yield a time period equivalent to a "maximum packet processing time allowed for processing each of said packets and determined corresponding to packet length" in accordance with the current formed relation of claim 1. Accordingly, it is respectfully submitted that the invention now defined by claim 1 is patentable over the

references.

Independent claim 8 now recites a "maximum packet processing time allowed for processing each of said packets and determined corresponding to packet length." For reasons along the lines discussed above with respect to claim 1, it is respectfully submitted that this is not suggested by the references.

Since the remaining claims that have been rejected depend from the independent claims discussed above and recite additional limitations to further define the invention, they are petantable along with their independent claims and need not be further discussed.

It is noted that this application has been amended to include four independent claims. Accordingly, an additional claim fee of $86 is being included in a remittance that is being submitted concurrently.

Respectfully submitted,

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